13.2.1 The RS Flip-Flop

The RS flip-flop has two inputs, R and S, and two outputs, Q and Q'. When R is high and S is low, the output Q is set to high; when R is low and S is high, the output Q is reset to low. If both R and S are high, the output Q is indeterminate.

13.2.2 Flip-Flops

Flip-flops are memory elements that store a single bit of information. They are used in digital circuits to provide temporary storage of data. There are different types of flip-flops, such as RS, JK, and D flip-flops.

13.3 Introduction

In this chapter, we will cover some fundamental aspects of digital circuits, including flip-flops and their applications.
If the AND input returns to 1 at a later time, the K input recog- nizes the AND input to be 1. The action holds Q = I. Assume the flip-flop is in the state Q = 1. If Q = 0, the K input now belongs to the lower NAND gate, which is ANDed to the top input of the lower NAND gate, which inputs X and Y. The Q = 0 output is fed to the top input of the lower NAND gate and the output of the lower NAND gate is the final output of the flip-flop.

Assume the flip-flop is in the state Q = 1. If Q = 0, the K input now belongs to the lower NAND gate, which is ANDed to the top input of the lower NAND gate and the output of the lower NAND gate is the final output of the flip-flop.

The two outputs are labeled SET and RESET. The two outputs are shown in the figure.
If we assume the flip-flop is in the state \( Q = 1 \), then a low \( S \) means a low \( Q \) will result in a low \( O \). We can describe the flip-flop as an active low set because a low input sets the flip-flop. By active low set, we mean that for a LOW input \( S \) to make \( Q \) change from 0 to 1, \( Q \) must be 0. The flip-flop diagram of Fig. 13.1 shows the NOR gate that makes the flip-flop change to \( 1 \) when \( S \) is 0. The flip-flop is an example of a basic digital circuit that uses a NOR gate.
Figure 13.4. The RS flip-flop.

The explanation is simple. If the clock input is zero, then both NAND outputs R and S have high outputs and \( S = R = 1 \), which means, from our

Independent of the R and S inputs, if the clock input is 1, the flip-flop state is J3.4 does just this. Its output assumes the state imposed by the set or reset

\[ \text{Truth table:} \\
\begin{array}{c|cc}
\text{Input} & R & S \\
0 & 0 & 1 \\
1 & 1 & 0 \\
\end{array} \\
\]

\[ \text{Diagram:} \\
\]

SEC 13.2 Flip-Flops
The D Flip-Flop

Shown in Fig. 13.5, if the PRESET input, \( P = 0 \), then \( Q = 1 \) immediatley while the CLEAR input, \( \overline{Q} = 0 \), and if the ENABLE input is high. The PRESET and CLEAR inputs are exclusive OR gates, and when the PRESET or CLEAR inputs are high, the flip-flop is forced to its stable state.

The PRESET input forces the flip-flop into its stable state, while the CLEAR input forces the flip-flop into its complementary stable state.

The D input is the data input. When the clock is high, the output of the D input is transferred to the flip-flop. When the clock is low, the output remains unchanged.

The output, \( Q \), is the complement of the D input when the clock is high. When the clock is low, the output remains unchanged.

The PRESET and CLEAR inputs are used to set or reset the flip-flop. When the PRESET input is high and the CLEAR input is low, the flip-flop is set. When the PRESET input is low and the CLEAR input is high, the flip-flop is cleared.
IEEE 1322 Logic Diagram Figure 137

This is an example of a gate D flip-flop, which is a basic digital circuit. The diagram shows the logic levels and connections for a D flip-flop. The figure includes a timing diagram and a truth table for the flip-flop's operation.

The flip-flops in the diagram are shown in active 'low' state. One flip-flop is active 'high', and the other is active 'low'. The diagram illustrates the setup and transition conditions for the flip-flops.

The truth table for the flip-flop is shown below:

<table>
<thead>
<tr>
<th>Clock (CK)</th>
<th>Data (D)</th>
<th>Qn</th>
<th>Qn+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The flip-flops are connected in a way that the output of one flip-flop is the input of another, creating a feedback loop. This is a typical configuration for a basic digital circuit.
A toggle or divide-by-two circuit can easily be made from an edge-triggered flip-flop.
The diagram shows the operation of a flip-flop circuit. The flip-flop is a primary storage element in digital electronics, used to store binary data. The diagram illustrates the logic states of the flip-flop under different conditions. The flip-flop has two inputs and one output, with the output being updated based on the inputs. The flip-flop circuit is essential in basic digital circuits and is used in various applications, including memory devices and digital logic gates.
13.2. The JK Flip-Flop

In general, the JK flip-flops are preferred over master/slave flip-flops because the JK flip-flops are protected from false transitions.
13.26 Flip-Flop Setup and Hold Times

Diagram in Fig. 13.17(d) shows the timing diagram in Fig. 13.15(a) and the timing sequence. The timing symbol is shown in Fig. 13.15(c) and the timing sequence is shown in Fig. 13.15(d). The diagram shows the relationship between the setup and hold times for the flip-flop. The setup and hold times are measured from the clock edge to the data input edge. The setup and hold times are critical for the proper operation of the flip-flop. If the setup or hold times are violated, the flip-flop may not function correctly.