configuration, but this term is somewhat misleading because the overall logic function is AND with positive logic; that is, the output on the common line connecting all the open collector gates is high only when all the open collector outputs are high; wired AND would be a better name. Two ordinary totem pole NAND gates would not work in the circuit of Fig. 12.30(b) because the high and low outputs would fight each other.

By a similar argument, two open collector AND gates (but not totem pole gates) with outputs connected together would implement the function $F = A \cdot B \cdot C \cdot D$. Notice also that the open collector configuration can be used to produce an output voltage greater or less than the 5-V supply to the open collector gates simply by changing the external voltage connected to the pullup resistor.

### 12.7.5 Three-State TTL Gates

The open collector gates just described have one disadvantage: They are much slower for a low-to-high output transition than the totem pole TTL gates. Consider what happens when the output goes from low to high. $Q_1$ is turned off, and the load capacitance $C_L$ must charge to the high output voltage. With totem pole TTL the charging path is from $V_{ee}$ through an active transistor $Q_1$, which has a very low impedance, typically less than 100 Ω, as shown in Fig. 12.31(a). But with an open collector gate, the charging path is from $V_{ee}$ through the external pullup resistance, which is usually 1 kΩ or more, as shown in Fig. 12.31(b). Thus, the charging time constant is much larger for the open collector gate. The external pullup resistance cannot be made much smaller because it would then draw too much current from the power supply when the output is low. Totem pole and open collector gates have the same speed for a high-to-low output transition because in either case a transistor ($Q_2$) is being turned on and $C_L$ discharges through $Q_2$ to ground. The three-state gate or tristate® (trademark of National Semiconductor) solves this problem by combining the speed of the totem pole TTL with the advantage of the open collector gate—allowing all the outputs to be connected together if desired. The solution, shown in Fig. 12.31(c), is called a three-state gate. There are three

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**FIGURE 12.29** Open collector TTL NAND gate.

**FIGURE 12.30** Open collector gate circuits.

**TABLE**

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possible output states: (1) output high with $Q_1$ off and $Q_4$ on, (2) output low with $Q_3$ on and $Q_4$ off, and (3) the disabled state with both $Q_2$ and $Q_4$ off and the output presenting a high impedance. (This is equivalent to the open collector gate with a high output.) In the circuit of Fig. 12.31(c) the output is made a high impedance by a positive input C ("control" or "enable"), which makes the output $\overline{C}$ of the inverter $\overline{C}$ low (almost ground), which turns on both diodes $D_2$ and $D_4$. Turning on $D_2$ turns off $Q_2$ because it limits the base voltage of $Q_2$ to a maximum of about 0.7 V, which is not enough to turn on both $Q_2$ and $Q_4$. Turning on $D_4$ turns off $Q_4$ for the same reason. But when $C$ is low, $C$ is high, both diodes are off and the circuit works in the usual way. To sum up, when the control input is low, the gate operates as a normal totem pole gate with its high speed; but when the control input is high, both totem pole output transistors are turned off and the output of the gate is a high impedance to ground.

Three-state gates can be connected like open collector gates, with all their outputs connected together to make a wired AND circuit.

A buffer amplifier is also available in a tristate form; it is called a tristate® or three-state buffer, and its schematic symbol is shown in Fig. 12.31(d). It is basically a solid-state switch for low currents. When the enable or control input is high, the input and output are connected together; but when the enable or control input is low, there is a high impedance between the input and the output.

Open collector gates and three-state gates are often used to drive "buses" in logic systems. A bus here means a number of wires used to carry information (in the form of bits) between various parts of the system: for example, from data input lines to a storage memory, from the memory to a computation unit, or from a computation unit to an output device, such as a printer or a cathode tube display. Many such paths exist in digital systems, especially in computers. Thus, to minimize the wiring complexities, we want to use the same bus to carry different sets of information. The use of three-state or open collector gates allows us to do this by connecting three-state outputs from input devices, memory, computation units, and output devices all to the same bus.

Suppose we wish to transfer digital data to a computer memory and have the bus usable for other purposes when the data are not being actually transferred to the memory. One solution to this problem is shown in Fig. 12.32 with open collector gates. With the open collector NAND gates, the output of each gate is connected to one line of the bus, which goes to the computer memory. We assume here for simplicity that the data are in the form of four-bit words or nibbles, $D_3D_2D_1D_0$, and that we therefore have four lines, one for each bit. Each bus line is tied to a positive supply voltage through its own external pullup resistor. Each data bit comes in to one input of a NAND gate, and the other inputs are all tied together to a READ DATA line. If the READ DATA line is low, all the open collector gate outputs are high regardless of the data inputs; that is, each gate presents a relatively high impedance to the bus line, as shown in Fig. 12.32(b). Thus, the bus line can be used for other data transmission—any bus line can be driven low by the output of another open collector TTL gate connected to the same bus line. However, if the READ DATA line is high, then the gate outputs are the complement of the data input, as shown in Fig. 12.32(c). The point is simply that when the READ DATA line is low, all the open collector gate outputs are high (high impedance to ground) and the bus lines are unaffected by the data input to the gates. The bus can then be used
Three-state outputs are often built right into the output of some gates and more complicated devices, such as flip-flops and A/D converters. For example, microprocessor-compatible devices have three-state outputs that can usually be directly connected to a microcomputer bus.

If the data bus in a computer is bidirectional, then the gates and other circuitry connected to the bus must be open collector or three state. For example, connections to the older PDP-8/E and PDP-11 output lines (the annibus and the unibus) must be open collector or three state. Most modern computers use three-state outputs.

### 12.7.6 General Comments on TTL

**Inputs:** A logic 0 or low input is ideally 0 V, but a typical TTL value is 0.2 V (V_{CE_{sat}} of the lower totem-pole transistor). A low input should be less than 0.8 V for reliable TTL operation. Each low input to TTL must sink approximately 1.6 mA (0.4 mA for LS TTL) of current because a low input turns on the input transistor, and the input is connected to the emitter. This 1.6-mA current is the emitter current of the input transistor of the TTL chip. Thus, the maximum impedance for the source of the low input is 0.8 V/1.6 mA = 500 Ω for TTL and 0.8 V/0.4 mA = 2 kΩ for LS TTL.

A logic 1 or high input is ideally the supply voltage (V_{cc} = 5 V for TTL), but a typical value is 3.6 V. A high input should be greater than 2.0 V for reliable TTL operation. The source of the high input need supply very little current, because a high input turns off the input transistor of the TTL chip. A typical current for a high input is 50 μA or less. A floating or unconnected TTL input will be equivalent to a high input because the input transistor is not conducting. Unused inputs should be tied either low (to ground) or high (to V_{cc} through a 1-kΩ resistance for reliable operation). A floating TTL input is not a reliable high because the open input voltage is usually around 1.4 V. Thus a small noise spike of 0.6 V or more would produce a low input.

**Outputs:** A logic 0 or low output is ideally 0 V, but a typical TTL value is 0.2 V, the collector emitter voltage across the saturated output transistor Q_3 between the output and ground. The resistance of this transistor is usually approximately 25 Ω. A low output can sink up to 16 mA in ordinary 7400 TTL (8 mA for LS TTL) and thus can drive ten TTL inputs (20 LS TTL inputs also) to a logical 0 or low level without the output rising above 0.4 V. The term fanout refers to how many similar gates can be driven by the output; we say the fanout of standard TTL is 10 (20 for LS TTL). The output of a standard TTL gate can sink up to 16 mA without its output voltage rising above 0.4 V. A TTL output can be shorted to ground but not to V_{cc}, because that would burn out the bottom transistor Q_3 in the totem pole output.

A logic 1 or high output is ideally V_{cc} = 5 V for TTL, but a typical value is 3.6 V, or approximately two diode drops below the supply voltage. The positive supply voltage is connected to the high output through a

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**FIG. 12.7** Logic Families

**FIG. 12.32** Open collector and three-state applications.

For transmission of other information. But when the READ DATA line is low, then the complement of the input data is fed onto the bus lines.

The data can also be fed onto the bus through three-state buffers, as shown in Fig. 12.32(d). If the ENABLE DATA (ED) line is low, the buffers act as open switches with a high output impedance and no data gets through to the bus. But if the ED line is high, the data is fed onto the bus. For example, if ED is high and EF is low, the D output will be fed onto the bus; if ED is low and EF is high, the F input will be fed onto the bus.
130-Ω resistance, a saturated output transistor, and a conducting diode. Because a high input to a TTL gate requires almost zero driving current, a high TTL output can drive a large number of TTL gates high. The fanout limitation occurs when the output is low. Special TTL gates called buffers are available with extremely high fanouts to drive a large number of gates. The 7437 NAND gate, for example, has a fanout of 30. Fanout capability usually is not a problem in small systems, but it can occur if one chip is used to reset a large number of chips by driving their inputs low.

The noise margin is a measure of how much the signal voltage must change in order to transform a logical 0 to a logical 1 as interpreted by the TTL gates—the larger the noise margin, the better. TTL manufacturers guarantee that any input about +2.0 V will be interpreted by the gate as a good high input, and any input below 0.8 V will be interpreted as a good low input. They also guarantee that the maximum high TTL output from the gate will be +2.4 V, and that the minimum low TTL output will be +0.4 V. The noise margin for these worst cases is thus 0.4 V.

A typical high TTL output is +3.6 V, so a −2.8-V noise spike would be required to change it to a “sure” low input of 0.8 V for another TTL gate. Similarly, a typical low TTL output is +0.2 V, so a +1.8-V noise spike would be required to change it to a “sure” high input of 2.0 V for another TTL gate.

Notice that a high input held at +5 V has a very large noise margin; a −4.2-V noise spike would be necessary to change it to a “sure” low input of 0.8 V. On the other hand, a low input held at ground would need only a +2.0-V noise spike to be interpreted as a “sure” high input of 2.0 V.

This is one reason TTL circuits are usually designed with active low inputs (ENABLE, RESET, etc.). With an active low input the normal (unused) input condition is thus high−5.0 V, obtained by connecting the input pin to +5 V through a 1-kΩ resistor. Then a huge (and improbable) −4.2-V noise spike on the input would be required to enable the input accidentally, whereas if the input were active high, it normally would be near ground, obtained by connecting a 1-kΩ resistor to ground (you can’t hard-wire it directly to ground because it would then be low permanently), and only a +2.0-V noise spike could accidentally enable it.

Active low inputs are also used because they save power. A pullup resistor to +5 V on a TTL input draws very low current (50 µA or less), but a pulldown resistor to ground would draw 1.4 mA for TTL or 0.4 mA for LS TTL.

If a low input drifts more positive, it would probably be interpreted as a high when it reaches approximately 1.4 V. But voltage levels between 0.4 V and 2.4 V should be avoided like the plague.

Consider a TTL gate with a high output; the bottom transistor Q3 in the totem pole output is off. If the ground voltage goes negative from a noise spike, Q3 may be turned on, thus producing a false low gate output. A negative spike of only −0.5 V on the ground lead can produce a false low output, so a reliable noise-free ground is absolutely essential.

A final comment concerns the $V_{cc}$ power supply: All TTL gates are designed to run off $V_{cc} = 5 V ± 0.25 V$. If $V_{cc}$ rises to 7 or 8 V (for example, by short-circuit failure of the voltage regulator chip), all the TTL gates may be permanently destroyed in milliseconds. The 1-kΩ resistor usually used between a TTL input kept high and $+V_{cc}$ protects the chip in case $V_{cc}$ increases.

### 12.7.7 Schottky and Low-Power Schottky TTL

The principal speed limitation in TTL logic is the delay caused in turning off the saturated “on” transistors. A saturated “on” transistor cannot be turned off until all the minority charges in the base region (electrons in the p-type base for the usual npn transistors) have diffused out of the base region, because in a saturated transistor there is essentially zero electric field in the base. In the Schottky and the low-power Schottky families all the transistors are prevented from ever saturating by connecting a Schottky diode between the base and the collector, as shown in Fig. 12.33(a). We recall that a Schottky diode turns on at approximately 0.3 V, and the transistor collector-base voltage must drop to approximately 0.2 V for the transistor to saturate. Thus, the Schottky diode turns on before the transistor can saturate. In other words, the excess base current necessary to saturate the transistor is diverted around the transistor through the diode when the diode turns on, thereby preventing transistor saturation.

![FIGURE 12.33 Schottky transistors](image)

It is very easy to add a Schottky diode to an npn transistor, as shown in Fig. 12.33(c). The aluminum contact to the base is simply extended to cover part of the n-type collector. The aluminum-base junction acts like a Schottky diode.

The low-power Schottky TTL series gates draw approximately one fifth of the power of standard TTL gates and have essentially the same speed and price. Thus the LS series TTL gates have replaced the standard TTL gates in all new TTL designs.

### 12.7.8 CMOS

CMOS stands for complementary metal-oxide semiconductor. CMOS gates use much less power than TTL gates but are much slower. CMOS circuits...
use both n-channel and p-channel enhancement MOSFETs in "complementary" pairs. Extremely low power consumption is achieved because power is consumed only when the circuit is switching states—not while the circuit is in the steady state. Other advantages include larger noise margins, relative immunity to temperature fluctuations, operation from +3 to 18 V supply, and a large fanout capability.

We recall that junction FETs or JFETs always must have the gate-channel junction reverse biased; if it is forward biased, the gate input will draw current and will be a low impedance. But with MOSFETs the gate is separated from the channel by an insulating layer of silicon dioxide, so the gate-channel voltage can be of either polarity and the gate input always has an extremely high input impedance. Plots of the drain current versus gate-source voltage for all four devices are shown in Fig. 12.34. Note that both types of enhancement MOSFETs need a nonzero gate-source voltage in order to conduct.

The basic operation of such complementary symmetry MOSFETs can be seen by considering the inverter circuit of Fig. 12.35. Notice that the output is taken from the two drains, which are connected together, and that the input is applied to the two gates, which are also connected together. Because the two enhancement MOSFETs are different types, one n-channel and one p-channel, it is impossible to forward bias both simultaneously so as to draw current from the power supply. Thus, no steady-state power is consumed (actually approximately 10 nW from leakage current) regardless of the logic state of the input. If the input is low (near 0 V), then the lower n-channel MOSFET is not conducting, but the upper p-channel MOSFET is conducting because its gate is negative with respect to its source. Thus, the output terminal is connected to the positive supply voltage through the upper (on, low-resistance) MOSFET, and the output is high, approximately the positive supply voltage. But, on the other hand, if the input is high (near the positive supply voltage), then the lower n-channel MOSFET is conducting because its gate is positive with respect to its source. The upper p-channel MOSFET is not conducting because its gate and source are at the same voltage. Thus, the output terminal is connected to ground through the lower (on, low-resistance) MOSFET, and the output is low, approximately 0 V.

A CMOS NAND gate and its truth table are shown in Fig. 12.36(a). Both Q1 and Q2 must be on to drive the output low; this output will be low only when inputs A and B are each high (near $V_{DD}$), which also turns off both Q1 and Q2. If both inputs are low (near ground), then Q3 and Q4 are both off—and Q1 and Q2 are both on; thus the output is high. If A is high and B is low, then Q1 is on and Q2 is on from A, Q3 is on, and Q4 is off from B. The output is high. If A is low and B is high, then Q1 is on and Q3 is off from A. Thus Q2 is off, and Q4 is on from B, which makes the output high. A CMOS NOR gate is shown in Fig. 12.36(b).
The following comments apply to all CMOS gates. A high state means a voltage level near the positive supply voltage \( V_{cc} \), and a low state means a voltage near ground. The boundary between high and low is approximately one-half the supply voltage. The supply voltage can be from 3 to 18 V, with the speed increasing with increasing supply voltage. The input impedance is typically \( 10^{12} \) \( \Omega \) in parallel with 5 pF, and the input current drawn is essentially zero (10\(^{-11}\) A typically) because all inputs go to the gates of MOSFETs, which are insulated from the rest of the circuit by the silicon dioxide layer between the gate and the channel of the MOSFET. The high output state means the output is connected to the positive supply voltage through an “on” MOSFET, and a low output state means the output is connected to ground through two “on” MOSFETs in series. The minimum high input should be approximately 0.7\( V_{DD} \); the maximum low, 0.3\( V_{DD} \) for reliable operation, although 0.5\( V_{DD} \) marks the difference between high and low.

Unused inputs must be connected either to ground or to \( V_{cc} \); they should not be left open. Because of their high impedance, the voltage of an open input may drift up and down, producing random 0 and 1 inputs. If an entire gate in a package is not used, all of its terminals should be grounded.

Because the input terminals have such a high impedance (high resistance and low capacitance) to ground, they are susceptible to damage from the buildup of static charge. The breakdown voltage of the SiO\(_2\) CMOS gate is approximately 70 V, and once broken down the CMOS device is usually permanently destroyed. Most CMOS gates have several input protection diodes built into their inputs, as shown in Fig. 12.37(a). The breakdown voltage is usually 25 V for the \( D_1 \) diodes, 60 V for \( D_2 \), and 100 V for \( D_3 \). These diodes will conduct whenever the input voltage is more than one diode drop above \( V_{cc} \) or more than one diode drop below ground. It should be pointed out that some CMOS gates such as the 4049 Inverter and the 4050 buffer contain only one input protection diode, as shown in Fig. 12.37(b).

Finally, although the steady-state power consumption is essentially zero because there is always a nonconducting enhancement MOSFET between the input and the gate, a surge or spike of current will be drawn from the supply when the circuit is switching from one state to another, because for a brief time interval both of the MOSFETs are on; the longer the input rise time, the longer the current spike lasts, and the greater the power dissipated. For moderate switching frequencies this represents a very low power con-
sumption on the order of microwatts, but as the switching frequency goes up, the average power consumption also goes up. Each time the output changes from 0 to 1, the output voltage changes from 0 to \( V_{ee} \), and the output capacitance to ground must charge up to \( V_{ee} \), requiring energy \( CV_{ee}^2/2 \). Thus the "switching" or "ac" power consumption is proportional to \( fC V_{ee}^2 \), where \( f \) is the frequency.

The fanout of CMOS gates is large because of the small input current one CMOS gate can typically drive 50 other CMOS gates.

The standard CMOS chips are numbered in the 4000 series; for example, 4011 is a quad-two-input NAND gate, 4007 is a quad-two-input NOR gate, and 4049 is a hex inverter. The 54C or 74C series is also CMOS and is typically 50% faster than the 4000 series; for example, a 74C00 is a quad-two-input NAND gate, and so on. Three-state CMOS gates are available, as in TTL. There are no open collector CMOS gates as there are in TTL, but the CMOS family does contain "analog switches" (which can conduct current in either direction), which are unavailable in TTL. One such analog switch is the 4051, which can be turned on or off by a voltage input that need supply essentially no current. Also, the switch input and output terminals can be interchanged just as for a mechanical switch.

### 12.7.9 Emitter-Coupled Logic (ECL)

The ECL family is the fastest, with propagation delays from 0.75 to 4 ns and operating frequencies up to several hundred megahertz. It is based on transistors in the common base configuration with the outputs taken off the emitters, hence the name. The transistors are prevented from ever saturating. The ECL family has a high fanout and operates from a negative supply voltage, \( V_{ee} = -5.2 \text{ V} \) or \(-4.5 \text{ V} \). Its principal disadvantage is that the difference between the two logic levels is very small: A logic low is \(-1.7 \text{ V} \), and a logic high is \(-0.9 \text{ V} \). Many different gates are available; the ECL family chips are numbered in the 10000 and the 100000 series.

### 12.7.10 High-Speed (HC) CMOS Family

The newest version of CMOS is the high-speed CMOS family or HC series. A high-speed CMOS quad NAND gate would be denoted 74HC00 and is logically equivalent to a 74LS00 or 7400 chip. The 74HCXX series combines the speed of the 74LSXX low-power Schottky TTL family with the low power consumption of the 74CXX CMOS or 4000 CMOS families. At this writing, as many chip types are available in the HC family as in either the LS TTL or TTL families. Thus most new designs use the HC family.

The high speed of the HC family is made possible by the smaller size of the active area of the chip. Supply voltages can range from 2 to 6 V; 5 V is recommended. Both 54HCXX (military, \(-55^\circ \text{C to } 125^\circ \text{C}\)) and 74HCXX

(incorporating, \(-40^\circ \text{C to } 85^\circ \text{C}\)) are available. The 74HCXX noise margin is not quite as good as for standard CMOS: minimum 3.15 V for a high input, and maximum 0.90 V for a low input.

The minimum high output is \((V_{ee} - 0.1 \text{ V})\), and the maximum low output is 0.10 V. HC D flip-flops can be clocked up to 30 MHz with a 15-pF load and 20 MHz with a 50-pF load, and the clock-to-Q output time is only approximately 25 ns.

As with any chip, the junction temperature \( T_1 \) inside the chip active material is given by

\[
T_1 = T_A + P_D \theta
\]

where \( T_A \) = the ambient temperature, \( P_D \) = the power dissipation in watts, and \( \theta \) = the thermal resistance in degrees Celsius per watt of the chip. \( \theta = 130^\circ \text{C/W} \) for most HC chips in a plastic DIP, and \( \theta = 100^\circ \text{C/W} \) for a ceramic DIP.

A few precautions are in order for (HC) CMOS.

1. The input signal should have a transition time of less than 500 ns (from \( 0.1V_{ee} \) to \( 0.9V_{ee} \)).
2. Unused inputs should be connected to \( V_{ee} \) or to ground.
3. The \( V_{ee} \) power supply leads should be well bypassed.
4. Check the flip-flop "hold time" requirement—the data must remain stable for a certain number of ns even after the active edge.
5. The minimum high input required is approximately 3.1 to 3.5 V (compared to 2.0 V for TTL). This may be a problem when driving 74HCXX with 74LSXX if extra output current is drawn from the 74LSXX output. (The CMOS input requires only nA or less.) A pullup resistor may be necessary on the 74LSXX output or a driver/buffer between the 74LSXX output and the 74HCXX input.
6. As we can see from Fig. 12.37, the output voltage should never be more positive than \( V_{ee} \) plus one diode drop, or else the output diode will conduct. Similarly the output voltage should never be more negative than one diode drop below ground.

To avoid burning out either regular 74CXX CMOS or 74HCXX high-speed CMOS chips, observe the following rules:

1. Store in conducting (black) foam, never white foam.
2. Handle chips should be laid leads down on a conducting surface (metal).
3. Ground soldering iron tips.
4. Turn off the power before either inserting or removing chips.
5. Be sure unused inputs are either grounded or wired to \( V_{ee} \). (Be careful of the high impedance "off" output of three-state outputs.)
6. In an extremely "noisy" electrical environment a 10-kΩ to 100-kΩ resistance in series with the input provides considerable protection at the expense of slightly lower speed.
12.7.11 Power Dissipation in CMOS Chips

The power dissipation is due to the steady dc leakage current (typically 1 nA or less) drawn from the $V_{ee}$ supply plus the transient dissipation due to charging and discharging the internal and external capacitances as the circuit changes output states. The transient power dissipation depends linearly on the switching or signal frequencies, the rise and fall times of the input, $V_{in}$ ($n = 2$), and the internal and external capacitances.

It can easily be shown that charging up a capacitance $C$ to a voltage $V_{cc}$ dissipates $W_R = CV_{cc}^2/2$ energy in the charging resistance. The energy stored in $C$ is also $CV_{cc}^2/2$ of course. Thus in charging $C$ through $R_L$ to a voltage $V_{cc}$, half the energy supplied by the input is stored in the electric field of the capacitance and half is converted into heat in $R_L$.

In discharging $C$ through $R_L$ the $CV_{cc}^2/2$ energy stored in the capacitance is all dissipated as heat in $R_L$. Thus, for each low-high-low transition, $2 \times CV_{cc}^2/2$ energy is dissipated as heat in $R$. Thus for a frequency $f$ the power dissipated as heat in charging and discharging $C$ is

$$P = f \times CV_{cc}^2$$

Table 12.12 contains a summary of the basic specifications of the various logic families.

12.8 INTERFACING

Connecting digital gates of different families to one another and to the "outside world," such as switches or lights, presents some special problems. These problems arise because of the different current and voltage requirements for the high and low logic states for the different families and the special requirements of the outside-world devices. For example, a low LS TTL input must sink approximately 0.4 mA of current, and a high TTL input need supply only $\approx 50 \mu$A of current. Either a high or a low input to a CMOS gate need supply negligible current, but the CMOS high-voltage level can be substantially higher than for TTL. The LS TTL and CMOS input and output characteristics are given in Table 12.12.

12.8.1 CMOS to TTL

If a CMOS gate output is to drive a TTL input, the main difficulty is that the low CMOS output cannot sink enough current for the TTL input. This occurs because the low CMOS output is connected to ground through an "on" MOSFET that may have a resistance of up to 500 $\Omega$. Thus, if the 1.6-mA sinking current for a good TTL low input flows into the CMOS output, the CMOS output voltage will rise to approximately $(1.6 \text{ mA}) \times (500 \Omega) = 0.8 \text{ V}$, which is the maximum voltage for a good low TTL input.
In other words, an ordinary CMOS low output cannot reliably drive a standard TTL input. Because a 74LS00 series TTL input must sink only about 0.4 mA, an ordinary CMOS gate can drive several low-power Schottky TTL gates. The high CMOS output of 5 V is fine for supplying a high TTL input.

The solution is to use a CMOS buffer (with a 5-V supply) between the ordinary CMOS gates and the TTL gates, to be driven as shown in Fig. 12.38(a). The 4049 CMOS hex inverter, for example, will drive two 7400 series TTL gates or eight 74LS00 series gates. If a larger fanout is required, the 74C906/907 CMOS open drain buffer can be used. This is analogous to the open collector TTL gate and requires an external pullup resistor, as shown in Fig. 12.38(b). The 74C906 can sink 8 mA when operated on $V_{cc} = 5$ V.

If the CMOS power supply voltage is greater than 5 V, the high CMOS output voltage level must be reduced to avoid destroying the TTL input. The solution is to use a 4049 or a 4050 CMOS buffer running off a 5-V supply, as shown in Fig. 12.38(c). Unlike TTL gates, the CMOS input of the buffer is not destroyed if the input voltage is higher than the buffer supply voltage. The CMOS buffer fanout for a 4049 or a 4050 is again two 7400 series gates or eight 74LS00 series gates.

**12.8.2 TTL to CMOS**

If a TTL gate is used to drive a CMOS gate, the main difficulty is that the 3.5-V TTL output high is barely high enough for a good high CMOS input, which really should be 4 V or more if the CMOS supply is 5 V. (The 74HC00 high-speed CMOS series typically uses a 5-V supply.) If the CMOS supply is 10 V, then a good high CMOS input is about 8 V, and the 3.5-V TTL high is far too low.

For 5-V CMOS the solution is to use an external pullup resistor to 5 V on the output of the TTL, as shown in Fig. 12.39(a). This makes the high TTL output 5 V. Either standard TTL or open collector TTL gates can be used in this way. For 10-V CMOS an open collector TTL gate can be used with the external pullup resistor going to a +10-V supply, as shown in Fig. 12.39(b). This makes the high TTL output 10 V. To get a good high output voltage equal to the external supply voltage, the pullup resistance should be small compared to the “off” resistance of the lower transistor in the output totem pole of the gate; this requirement is easy—any value under 10 kΩ is fine. To get a good low output voltage, the pullup resistance should be larger than the “on” resistance of the lower transistor, which is several hundred ohms at most. The larger $R$ is, the larger the rise time will be, so values from 1 to 3 kΩ are used. Or an npn transistor can be used as shown in Fig. 12.39(c). If the TTL output is low, then $Q$ is off and the input to the CMOS input is high (about 10 V). If the TTL output is high, then $Q$ is on (saturated) and the CMOS input is low (about 0.2 V). Notice that the transistor inverts the output of the TTL gate; in other words, the transistor acts as an inverter.

**12.8.3 TTL to Outside World**

Because a TTL output low can sink 16 mA (7400 series), or 4 mA (74LS00 series) and a TTL output high can only supply 1 or 2 mA, it is generally best to turn on an outside-world device such as a lamp or a relay with a low TTL output. A TTL gate can turn on an LED, for example, with the circuit of Fig. 12.40(a). When the LED is on, the voltage drop across its terminals...
SEC. 12.8 Interfacing

connected across the relay coil to prevent excessive ringing, which otherwise would occur when the current changed suddenly through the inductance of the relay coil. Without the diode the ringing can produce voltages larger than \( V_{cc} \), which could destroy the gate. When the output of the TTL gate goes low, the relay draws current and the relay switch flips. Notice that a large current can either be turned on or off this way, depending on how the relay switch is connected. If the relay operates off a voltage higher than the 5-V TTL supply voltage, then an open collector TTL gate can be used as shown in Fig. 12.40(c), but the gate output must be able to withstand the higher supply voltage. Again, the diode is necessary to prevent ringing.

The low-power Schottky series of TTL gates can sink only up to 4 mA, so a higher current driver of some kind must be used between the LS gate and the load, as shown in Fig. 12.40(d). The 7404, 7406, or 7437 can be used.

To drive higher current loads (e.g., a large lamp) from TTL gates, we can use an external transistor, as shown in Fig. 12.40(e). The low TTL output will turn on the pnp transistor whose collector current is the load current. The resistance between the gate output and the transistor base is necessary because when the transistor is on, its base voltage will be about 4.4 V, which is considerably higher than the low gate output of only 0.2 V. Thus, the base current flowing through \( R \) must produce a drop of 4.2 V. If the load current with the transistor on is 100 mA, for example, and the transistor \( h_{fe} = 50 \), then the base current will be \( I_b = I_c/h_{fe} = 100 \text{ mA}/50 = 2 \text{ mA} \). Thus, from Ohm’s law \( R = 4.2 \text{ V}/2 \text{ mA} = 2.1 \text{ k}\Omega \). If \( R \) is larger than this value, the base current will be less and the load current will be too small. If \( R \) is smaller, the base and load currents will be larger, but too large a base current might exceed the current sinking capability of the low TTL output.

An npn transistor can also be used, as shown in Fig. 12.40(f). A high output will turn on the transistor, and current will flow through the load. The two resistances can be calculated when the load current is known. Notice, however, that the transistor base current can never be greater than the maximum current the high TTL output can supply, usually about 2 mA. Thus, for a transistor dc current gain of \( h_{fe} = 50 \), the maximum load current will be 100 mA. For such a case \( R_1 = (3.5 \text{ V} - 0.6 \text{ V})/2 \text{ mA} = 1.45 \text{ k}\Omega \). The resistance \( R_2 \) is necessary for noise immunity. The low TTL output might rise up to 0.8 V, which would turn on the transistor if \( R_2 \) were much larger than \( R_1 \). Usually, \( R_2 = R_1 \), which robs the transistor of some base current drive but provides better noise immunity. A larger current load could be driven by using a Darlington configuration or a super beta transistor with exceptionally high dc current gain.

Large ac current loads can also be driven with a solid-state relay turned on by a TTL output. The solid-state relay is basically an optically coupled triac that can switch up to 40 A at 115 V ac. Whenever large currents are

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**FIGURE 12.40** TTL to outside world devices.
switched on and off suddenly, large voltage transients and ringing oscillations are produced that can often create havoc in adjacent circuitry. One of the best ways to prevent this is to use a zero-crossing relay to switch the currents. Such relays essentially wait until the 115-V ac current reaches zero before they open or close, thereby minimizing the transient effects.

12.8.4 CMOS to Outside World

A CMOS high output can supply or “source” only about 1 mA of current, because the positive supply voltage is connected to the high output through an “on” MOSFET whose resistance is about 500 Ω. Thus, if 2 mA is drawn from a high CMOS output, the voltage will drop from 5 to 4 V. This severely limits what outside-world loads can be driven. A low CMOS output can sink only about 1 mA of current because the low output is connected to ground through an “on” MOSFET. Thus CMOS outputs can operate outside-world loads only if they draw or sink less than approximately 1 mA; this means, for example, that a CMOS output cannot drive even a single LED. It can turn on another MOSFET or a small transistor but not a large power transistor. The usual solution is to use a CMOS buffer such as the 4049 or 4050, which can source and sink more current, as shown in Fig. 12.41(a). The current that can be sourced or

![CMOS to outside world devices](image)

sunk depends strongly on the supply voltage, the currents increasing with increasing supply voltage. For example, the 4050 hex noninverting buffer can sink 5 mA at 5 V, 12 mA at 10 V, and 40 mA at 15 V.

The resistance $R$ is calculated from Ohm’s law in the usual way. For example, for driving an LED, for a 10-mA current, $R = (V_{ce} - 1.7) / 10$ mA. If $V_{ce} = 10$ V, then $R = 830$ Ω.

In all CMOS interfaces we should remember that the output voltage from the 4049 or 4050 buffers are $V_{ce}$ and 0 V for the logic high and low levels, respectively.

Special CMOS chips are available to drive larger loads. For example, the 74C908/918 is a dual CMOS 30-V relay driver and is shown in Fig. 12.41(b). It can source 250 mA at a 3.5-V output with $V_{ce} = 5$ V and can withstand up to 30 V across its output. It is useful in driving relays, lamps, and other devices.

12.8.5 LED and LCD Displays

It is often necessary to display numerical and verbal information so that it can be read by a human being. The general method for displaying a binary word (straight binary, or BCD, or ASCII, etc.) is shown in Fig. 12.42(a). A decoder/driver circuit converts the binary input into the proper electrical signals required by the display. Both LED and liquid crystal displays (LCD) are popular. LEDs are best in dim ambient light, while LCDs are best in bright ambient light. LEDs are usually red but are available in green, blue, and yellow. LCD displays use considerably less power than LED displays and are ideally suited to CMOS circuitry in portable applications. To save power, it is common to multiplex the LED display, which means to energize one digit at a time in rapid sequence. The slow response of the human eye (dc to ~25 Hz) makes all the digits appear to be continuously lit.

A typical seven-segment LED is shown in Fig. 12.42(b). The seven segments are denoted by lower case letters, a...g. A popular TTL BCD to seven-segment LED decoder/driver chip is the 7447 which is shown in Fig. 12.43. When a particular 7447 output pin goes low (e.g., pin a), then the corresponding LED element lights up. For example, to display the number seven, the LED elements a, b, and c are lit up, and the other elements d, e,
Other displays are also available such as the $5 \times 7$ dot LED display which can display many more characters than the seven-segment LED display. Many modern display units contain both the LED display and the decoder/driver circuitry. One such display is the HPDL-2416 which is an intelligent four-character alphanumeric (both letters and numbers) display in a DIP, including on-board CMOS memory, ASCII decoder, multiplexing, and driver circuitry.

### 12.8.6 Switch and Comparator Input to TTL and CMOS

We usually feed information into a digital circuit (or "input" the circuit) by typing on a keyboard or by having the analog information from a transducer (a thermistor or photocell, etc.) converted into digital form. The specifics of A/D conversion will be covered in Chapter 15.

High or low inputs can be supplied to a TTL gate or a CMOS gate with the pullup circuit of Fig. 12.44(a). When the switch is open, the input is

\[ V_{in} = +5 \text{ V} \]

when the switch is closed, the input is ground. The closed switch can obviously easily sink enough current for a good low TTL input. The value of the resistance $R$ is not critical—several thousand ohms for TTL and perhaps 10 kΩ for CMOS. The $V_{th}$ voltage can be higher than 5 V if the CMOS gate runs off of a voltage greater than 5 V. It is theoretically possible to use a pulldown resistor, as shown in Fig. 12.44(b), but there are three disadvantages. First, if the supply voltage ever exceeds 5 V for TTL, the TTL gates may be destroyed when the switch is closed. Second, the pulldown resistance must be fairly low to obtain a good low TTL input. For example, to keep the low input below 0.4 V, the resistance must be less than 80 Ω because the sinking current for a TTL low is 1.6 mA or less than 1 kΩ for LS TTL. Third, when the switch is closed to produce a high input,
a large current is drawn from the supply: \( I = \frac{5 \text{ V}}{250 \Omega} = 20 \text{ mA} \). This pulldown circuit should be avoided for TTL inputs, but it can be used for CMOS. \( R \) can be much larger than 250\( \Omega \) in CMOS circuits.

Finally, mechanical switches are almost never used to supply high and low logic inputs to digital gates because they "bounce" open and shut (for approximately 10 ms) when they are closed. The remedy is the "bounceless" switch, described in Section 12.8.7.

A comparator can drive a TTL circuit, as shown in Fig. 12.45(a). The output of many comparators is of the open collector type, so a pullup resistor is used to +5 V for driving TTL and to \( V_{cc} \) for CMOS. In Fig. 12.45(b) the resistance \( R' \) is necessary to limit the current through the CMOS protection diodes. The circuits of Fig. 12.45(a) and (b) are suitable for a comparator that runs between a positive supply voltage and ground, because then the high comparator output provides a suitable TTL or CMOS high, and a low comparator output is essentially at ground, which provides a good low for both TTL and CMOS. But if a bipolar or CMOS op amp is used as a comparator, its output can swing from +13 V to +15 V high to −13 V to −15 V low, and the low output can destroy the TTL gate input circuitry. A protective diode with a 100-\( \Omega \) current-limiting resistor [see Fig. 12.45(c)] prevents the low from going below approximately −0.6 V. At this writing most experimentalists use comparators that swing from a positive voltage to near ground, so this is not a real problem. Another way of driving TTL is to use the comparator output to turn on an npn transistor, as shown in Fig. 12.45(d). A positive comparator output turns on \( Q \) and thus provides a low input of 0.2 V to the TTL gate. A negative comparator output turns \( Q \) off and provides a high TTL input of 5 V. Thus the transistor acts as an inverter. The protective diode is necessary to prevent the negative comparator output from exceeding the maximum base emitter breakdown voltage (typically 7 V) of \( Q \). The resistance \( R \) limits the base drive to \( Q \).

For example, for a good low, \( Q \) should be saturated and its collector voltage will be 0.2 V. Thus, \( I_1 = \frac{(5 \text{ V} - 0.2 \text{ V})}{3 \text{ k}\Omega} = 1.6 \text{ mA} \), and \( I_2 = 1.6 \text{ mA} \) for the low sinking current for a good TTL low. Thus, \( I_c = 3.2 \text{ mA} \), and the base current is \( I_b = I_c / h_{FE} = 3.2 \text{ mA} / 100 = 32 \text{ \mu A} \). When \( Q \) is saturated, its base voltage will be approximately 0.7 V and thus \( R = \frac{(13 \text{ V} - 0.7 \text{ V})}{0.032 \text{ mA} = 384 \text{ k}\Omega} \). This is a maximum value for \( R \). To ensure saturation of \( Q \), we would use a smaller value for \( R \).

![Figure 12.45 Comparator/TTL-CMOS interfacing.](image-url)
12.8.7 The Bounceless Switch

A switch can be used to supply high or low logic inputs to digital gates. But most mechanical switches such as ordinary toggle switches and microswitches “bounce” when they are closed because of the mechanical bouncing of the switch contact inside the switch. The result is an erratic series of pulses approximately 1-10 ms long, as shown in Fig. 12.46(a). The low propagation time of TTL gates (typically 10 ns) can be used to make a “bounceless” switch, as shown in Fig. 12.46(b). The basis of this debouncing circuit is that the propagation time of the gate is much much less than the bounce period of the mechanical switch. The output of each NAND gate is fed back to the input of the other NAND gate. If the switch is flipped to the up position at \( t = 0 \), then \( A \) is set low at \( t = 0 \); and 10 ns later, the output \( C \) of the top NAND gates goes high, and the \( A' \) input of the lower NAND gate also goes high at \( t = 10 \text{ ns} \). But the two inputs of the bottom NAND gate are both high now, so after 10 ns more have elapsed, the output \( C \) of the lower NAND gate goes low from the NAND truth table, which means the other (B) input to the top NAND gate goes low at \( t = 20 \text{ ns} \). If the switch bounces open (thus changing \( A \) from low to high), after \( t = 20 \text{ ns} \) the output \( C \) of the top NAND gate will remain high because its \( B \) input is held low. Thus, if the switch mechanical bounce period is greater than the two propagation times (20 ns), the \( C \) output will go high and remain high even if the switch bounces open and shut. Basically all such switches in logical systems are debounced.

In digital systems the mechanical switch is often replaced by the output of a gate, as shown in Fig. 12.47(a) and (b). This technique is often used to set or reset a counter or other device with a low power pulse longer than 20 ns.

### PROBLEMS

1. Count from \( 30_{10} \) to \( 50_{10} \) in (a) binary, (b) octal, and (c) hexadecimal.

2. \( (10110)_2 = \binom{?}{10} \); \( (306)_8 = \binom{?}{10} \); \( (3F2)_{16} = \binom{?}{10} \).

3. \( (49)_{10} = \binom{?}{2}; (49)_{10} = \binom{?}{8}; (49)_{16} = \binom{?}{10} \).

4. \( (101011)_2 = \binom{?}{8}; (37)_8 = \binom{?}{2} \).

5. \( (11010011)_2 = \binom{?}{10}; (101011)_2 = \binom{?}{8} \).

6. \( (63)_{10} = \binom{?}{2}; (10110111)_{20} = \binom{?}{10} \).

7. The parity of \( 10110101 \) is \( \square \). The parity of \( 10111010 \) is \( \square \).

8. How many binary functions do two binary variables have? Three binary variables? Four binary variables?

9. Write the truth tables for the following functions of two binary variables: \( \text{AND, NAND, OR, NOR, NOT, XOR, XNOR} \). Sketch the standard gate symbol for each function.

10. Diagram how you would implement the following functions using (a) only NAND gates, (b) only NOR gates.

- \( F = A \cdot B + A' \cdot B' \)
- \( F = A + B \)
- \( F = A \cdot B \)
- \( F = A \cdot B' \)
- \( F = A' \)

11. Enter the following data into the circuit and find the output:

   - Input data: \( 101010101011001 \)
   - Output data: \( 0101010101010101 \)
12. Write the truth table for \( P \) in terms of \( D_3, D_2, D_1, D_0 \). What is \( P \) called?

\[
\begin{array}{c|cccc}
D_3 & D_2 & D_1 & D_0 & P \\
\hline
1 & 1 & 0 & 0 & 1 \\
1 & 1 & 0 & 1 & 1 \\
1 & 0 & 1 & 0 & 1 \\
1 & 0 & 1 & 1 & 1 \\
0 & 1 & 0 & 0 & 1 \\
0 & 1 & 0 & 1 & 1 \\
0 & 0 & 1 & 0 & 1 \\
0 & 0 & 1 & 1 & 1 \\
\end{array}
\]

13. Write a circuit diagram to realize an XOR gate using only NAND gates. Use \( A \oplus B = \overline{A \cdot B} + \overline{A} \cdot \overline{B} \).

14. Repeat Problem 13, using only NOR gates.

15. Write a circuit diagram to realize an XOR gate using only NAND gates. Using \( A \oplus B = (A + B) \cdot (A \cdot B) \).

16. Repeat Problem 15, using only NOR gates.

17. Explain why a 7400 low input must sink current.

18. Explain why an open 7400 input acts like a high input.

19. Explain what is meant by a totem pole output.

20. Explain why a high output in a TTL totem pole circuit cannot supply more than about 10-20 mA of current to an LED.

21. Explain how much current a low output in a TTL totem pole circuit can sink.

22. Explain why a low TTL output is approximately 0.2 V and a high TTL output is approximately 3.5 V.

23. Explain what an open collector gate is.

24. Write the truth table and the circuit for the realization of the function \( F = (A \cdot B) \cdot (C \cdot D) \), using only two open collector gates and a pullup resistor.

25. Repeat Problem 21 for the function \( F = A \cdot B \cdot C \cdot D \).

26. Briefly summarize the high- and low-voltage requirements for TTL gates.

27. Discuss the problems and solutions for connecting a CMOS output to a TTL input.

28. Repeat Problem 24 for a TTL output to a CMOS input.

29. Discuss how TTL and CMOS outputs can drive high current "outside world" loads.

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**CHAPTER 13**

**Basic Digital Circuits**

13.1 **INTRODUCTION**

In this chapter we consider some relatively simple digital circuits, many of which are available in a single chip. We consider flip-flops, which are the basic building blocks of all memory systems, counters, conversion from serial to parallel data, and vice versa; the transmission of digital data; arithmetic operations on binary numbers; and various other circuits. We assume positive logic: a high voltage level is a 1, and a low voltage level is 0.

13.2 **FLIP-FLOPS**

A *flip-flop* is essentially any circuit with two output terminals and two stable voltage states (one higher than the other) for each terminal. It is thus ideal for storing binary digital information, either data or instructions. It usually has several input terminals, such as SET, RESET, clock, and DATA, as will be explained shortly. It can be switched very quickly from one stable state to the other with an external pulse.

### 13.2.1 The RS Flip-Flop

The basic idea of a flip-flop can be seen from the discrete component circuit of Fig. 13.1(a). There is exact symmetry between the two sides of the circuit, so one might conclude that each transistor will conduct equally (i.e., have the same collector current). We will now show that one transistor will always be on and the other always off because of the \( R_1 \) and \( R_2 \) resistor voltage dividers, which couple the collector of one transistor to the base of the other transistor. Suppose each transistor is conducting equally. There will always be a voltage fluctuation due to noise at the bases. Suppose the base of \( Q_2 \) goes slightly more positive. Then \( Q_2 \) will draw more collector current, and the voltage at the collector will decrease (i.e., become less positive). The fraction \( R_1/(R_1 + R_2) \) of this drop in the collector voltage is applied to the base of \( Q_1 \), thus turning off \( Q_1 \) more. \( Q_1 \) draws less collector current, and its collector voltage rises (i.e., becomes more positive). A